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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,883	02/20/2004	David James Seal	550-509	4228

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/781,883	SEAL ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 January 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-33.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

RICHARD L. ELLIS
PRIMARY EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: Applicant has argued that the mapping Examiner made of the address decode logic in paragraph 5 of Qureshi does not properly map upon the claimed limitation of a decoder configured to decode program instructions. Examiner will conceed that the Applicant is correct in this regard, and that the address decode logic that the Examiner mapped to does not decode program instructions. However, Examiner still asserts that there is a decode which does this in Qureshi, as the limitations of the claim require that the instruction decoder decode program instructions, and can be operable in both modes disclosed. Therefore, if Qureshi does perform the rest of the claimed invention, Examiner believes it is a fair assertion to say that Qureshi has this decoder, and in addressing the rest of the Applicants remarks, Examiner will show how Qureshi does this.

Applicant has next argued that the difference between big endian and little endian storage are different ways of storing data, and not different instruction sets, and thus what Qureshi teaches is two modes of addressing, and not two different instruction sets. However, assuming the Applicants interpretation for the sake of argument, Examiner notes that the two subsets claimed are not necessarily different subsets, because unless the two are claimed as distinct, there is no requirement to read them as the same subset, therefore, even in Applicant's interpretation, the Examiners position is valid, as what Qureshi teaches (in Applicants interpretation) is two types of instructions in an instruction set, with a common bit-length (Examiner did note this amendment in the previous amendment, and Examiner notes that despite storing the instructions in a different way, they are the same length, therefore Qureshi reads on the limitation), and after addressing the different ways they are stored, can be arranged to form identical instructions, which is what has been claimed.

Applicant has made remarks towards Qureshi not teaching that a subset of the instructions fall into this category, however, a subset is a term which can encompass all, none, or part of a set, thus, in Qureshis case, the subset of instructions with a common bit length and identical bits after the compensation is the entire set, and if Applicant intends to argue on the basis that his claimed invention is not this way for every single instruction (which Examiner believes may be the case), then it needs to be made clear that the word "subset" is not referring to the whole set.

Additionally, Examiner would like to remark on the different instruction set remarks from above. If any instruction set is said to be the instruction set architecture, then different instruction sets have different opcodes, difference formatting, and so on. Therefore, in the claimed invention, when saying that when you have two instruction sets, and when compensating for their storage differences, are identical in every way, and perform the exact same operation, Examiner would argue that this is exactly what Qureshi does, as Examiner does not believe that for two different instruction sets, you can rearrange the bits such that everything is identical in every case (leading back to the subset discussion), because this would suggest that the instruction sets are the same, thus further supporting the Examiners current rejection of the claims, because as far as the Examiner can determine, Qureshi does exactly what is being claimed: It can take two different pieces of data stored in different ways, it can compensate for these differences, and afterwards, the exact same instruction is the result, both of which do the exact same thing, which is what is being claimed as best as Examiner can determine, therefore Examiner believes that his rejection is proper.